

Product Specification

2.5Gb/s Short-Wavelength GBIC Transceiver

FTR-8519-3-2.5

Product Features

- Up to 2.125 Gb/s bi-directional data links
- 850nm VCSEL Laser Transmitter
- “Smart “ Digital Diagnostics Functions
- Extended Operating Temperature Range (-10°C to +85°C)
- Extended Power Supply Voltage (Operate at 3.3V and 5V)
- Hot-Pluggable (complies with GBIC specification Rev. 5.4)
- Fully metallic enclosure for low EMI
- Low power dissipation



Applications

- 2.125Gb/s Fibre Channel
- Dual Rate 1.06 / 2.125 Gb/s Fibre Channel

Finisar’s FTR-8519-3-2.5 2.5Gb/s 850nm GBIC transceivers comply with GBIC Specification Revision 5.4¹. They are compatible with Gigabit Ethernet as specified in IEEE Draft P802.3z/D5.0² and 1x/2x Fibre Channel FC-PI 10.0³. Additional real time diagnostic functions are also available via the 2-wire serial bus specified for Module Definition “4” GBICs. For details, see Finisar Application Note AN-2025, “Using the Finisar GBIC I²C Test/Diagnostics Port”⁴.

I. Pin Out

Pin Name	Pin #	Sequence
RX_LOS	1	2
GND	2	2
GND	3	2
MOD_DEF(0)	4	2
MOD_DEF(1)	5	2
MOD_DEF(2)	6	2
TX_DISABLE	7	2
GND	8	2
GND	9	2
TX_FAULT	10	2
GND	11	1
-RX_DAT	12	1
+RX_DAT	13	1
GND	14	1
V _{CC}	15	2
V _{CC}	16	2
GND	17	1
+TX_DAT	18	1
-TX_DAT	19	1
GND	20	1

Table 1. GBIC to host connector pin assignment

“Sequence” indicates the order in which pins make contact when the device is hot plugged.

Also see “Table 3: Signal Definitions” in the GBIC Specification Revision 5.4.¹

II. +5/3.3V Volt Electrical Power Interface

Finisar GBICs have an extended power supply voltage range of 3.15V to 5.5V as described in Table 2. The GBIC specification calls for a range of 4.75V to 5.25 volts. The 6V maximum voltage is not allowed for continuous operation, however, TX_FAULT and TX_DISABLE circuitry in Finisar GBICs will function at 6V.

+5/3.3 Volt Electrical Power Interface						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Supply Current	I_s		190	250	mA	
Maximum Voltage	V_{max}			6	V	
Surge Current	I_{surge}			+30	mA	Hot plug, above steady state current.
Input Voltage	V_{cc}	3.15	3.3, 5	5.5	V	Referenced to GND. 3.3V & 5V compatible.

Table 2. +5/3.3 Volt electrical power interface

III. Low Speed Signals

RX_LOS, TX_DISABLE, and TX_FAULT are TTL signals as described in Table 3. MOD_DEF(1) (SCL) and MOD_DEF(2) (SDA), are open drain CMOS signals (see section VI, “Serial Communication Protocol”). Both MOD_DEF(1) and MOD_DEF(2) must be pulled up to host_Vcc. If host_Vcc is 3.3V, then they must be pulled to 3.3V. If host_Vcc is 5V, do not pull the MOD_DEF pins to 5V.

For more detailed information, see sections 5.3.1 – 5.3.8 in the GBIC Specification Rev. 5.4¹.

Low Speed Signals, Electronic Characteristics						
Parameter	Symbol	Min	Max	Units	Notes/Conditions	
GBIC Output LOW	V_{OL}	0	0.5	V	4.7k to 10k pull-up to host_Vcc, measured at host side of connector	
GBIC Output HIGH	V_{OH}	host_Vcc - 0.5	host_Vcc + 0.3	V	4.7k to 10k pull-up to host_Vcc, measured at host side of connector	
GBIC Input LOW	V_{IL}	0	0.8	V	4.7k to 10k pull-up to Vcc, measured at GBIC side of connector*	
GBIC Input HIGH	V_{IH}	2	Vcc + 0.3	V	4.7k to 10k pull-up to Vcc, measured at GBIC side of connector*	

*Note V_{IH} and V_{IL} are the same for both 5V and 3.3V operation

Table 3. Low speed signals – electronic characteristics

Low Speed Signal Parameters						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
RX_LOS Assert Level	--		-25.5		dBm	
RX_LOS Deassert Level	--		-23		dBm	
RX_LOS Hysteresis	--		1.5		dB	
RX_LOS Assert Delay	t_loss_on		44	100	μsec	From detection of loss of signal to assertion of RX_LOS
RX_LOS Negate Delay	t_loss_off		44	100	μsec	From detection of presence of signal to negation of RX_LOS
TX_DISABLE Assert Time	t_off		5	10	μsec	Rising edge of TX_DISABLE to fall of output signal below 10% of nominal
TX_DISABLE Negate Time	t_on		63	1000	μsec	Falling edge of TX_DISABLE to rise of output signal above 90% of nominal
TX_DISABLE Reset Time	t_reset	10			μsec	TX_DISABLE HIGH before TX_DISABLE set LOW
TX_FAULT Initialize Time	t_init			300	msec	From power on after VCC > 3.15 V
TX_FAULT Assert Time	t_fault			100	μsec	From occurrence of fault (output safety violation or VCC < 3.15V)

Table 4. Low speed signal parameters

IV. High Speed Electrical Interface

All high-speed PECL signals are AC-coupled internally.

High Speed Electrical Interface						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Data Input Voltage	V _{in}	650		2000	mV	PECL differential peak - peak
Data Output Voltage	V _{out}	370		2000	mV	PECL differential peak - peak
Duty Cycle	--		50		%	
PECL rise/fall	T _r , T _f		120	175	psec	20% -80% Differential
Bit Error Rate	BER			10 ⁻¹²	error/sec	PRBS 2 ⁷ - 1 test data pattern
Tx Input Impedance	Z _{in}		75		ohm	
Rx Output Impedance	Z _{out}		75		ohm	

Table 5. High-speed electrical interface

V. Optical Parameters

Optical Parameters						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Transmitter Center Wavelength	λ_c	820	850	860	nm	
Transmitter Spectral Width (RMS)	$\Delta\lambda$		0.5		nm	RMS
Transmitter Optical Output Power	P_{out}	-9.5	-7	-5	dBm	Average Power
Optical Modulation Amplitude	OMA	0.196			mW	Allows smaller ER at higher average power
Transmitter Eye Opening	--	60			%	Conforms to IEEE 802.3 and Fibre Channel Eye Masks
Total Transmitter Jitter Contribution	TJ_{TX}		45	119		Measured at TP2, as defined in GBE standard
Total Receiver Jitter Contribution	TJ_{RX}		50	122		Measured at TP4, with loopback from Tx
Optical Input Wavelength	λ_{in}	820		860	nm	
Optical Receiver Sensitivity <=1.25 Gb/s	R_{XSENS} (1X)		-22	-20.5	dBm	BER < 10^{-12} w/ PRBS $2^7 - 1$ test data pattern @ 1.25Gb/s
Optical Receiver Sensitivity >1.25Gb/s	R_{XSENS} (2X)			-15	dBm	BER < 10^{-12} w/ PRBS $2^7 - 1$ test data pattern @ 2.125Gb/s
Stressed Receiver Sensitivity @1.25Gb/s				-13.5	dBm	As defined in GBE standard

Table 6. Optical parameters

VI. General Specifications

General						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Data Rate	BR		1.0625, 1.25, 2.125, 2.5		Gb/sec	1x/2x Fibre Channel, IEEE 802.3 Compatible
Fiber Length on 50/125µm 500MHz-km Fiber	L			550 (300)	m	@1.0625Gb/s (@2.125Gb/s)
Fiber Length on 62.5/125µm 200MHz-km Fiber	L			300 (150)	m	@1.0625Gb/s (@2.125Gb/s)

Table 7. General specifications**VII. Environmental Specifications**

Note that the GBIC Specification requires an ambient temperature range of 0 to 50°C. Finisar GBICs have an extended range from -10°C to +85°C case temperature as specified in Table 8.

Environment						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Operating Temp	T _{op}	-10		85	°C	
Storage Temp	T _{sto}	-40		85	°C	
Eye Safety	--					CDRH and IEC-825 Class 1 Laser Product

Table 8. Environmental Specifications

VIII. Serial Communication Protocol

All Finisar optical GBICs are ‘Module Definition “4”’ and support the 2 wire serial communication protocol outlined in the GBIC Specification¹. These GBICs use an Atmel AT24C01A 128 byte E²PROM (with an address of 1010000X). For details on interfacing with the E²PROM, see the Atmel data sheet titled “AT24C01A/02/04/08/16 2-Wire Serial CMOS E²PROM.”⁵

All Finisar optical GBICs also incorporate a microcontroller that monitors system parameters such as received optical power, laser current, laser temperature, and, in the case of 1310nm parts, transmitted power. The microcontroller I²C address is 1010111X, so it won’t conflict with the AT24C01A. For a complete description of how to use Finisar’s extended features, see Finisar’s Application Note AN-2025: “Using the Finisar GBIC I²C Test/Diagnostics Port.”⁴

CAUTION: The microcontroller implements the Philips I²C protocol including clock stretching. For details, consult the Philips I²C-Bus Specification. Clock stretching allows a fast master to communicate with a slow slave device, and it requires that the host monitor the clock line every time it releases the line high. If a host does not implement clock stretching (drives the bus blind), it must run the clock below 8kHz, so that Finisar’s microcontroller has time to process instructions. If clock stretching is supported, the clock may be run at up to 100kHz.

I ² C Timing Requirements						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Atmel I ² C Clock Rate	C _{atmel}	0		100,000	Hz	Bus can be driven blind. FTR-8519P-5A only.
Finisar Microcontroller I ² C Clock Rate	C ₁	10		100,000	Hz	Host must support clock stretching. Microcontroller times out if C < 10Hz.
Finisar Microcontroller I ² C Clock Rate	C ₂	10		8000	Hz	Bus can be driven blind. Microcontroller times out if C < 10Hz.

Table 9. I²C timing requirements

IX. Mechanical Specifications

Finisar GBICs conform to the mechanical specifications outlined in the GBIC Specification Revision 5.4, Section 6¹.

Insertion, Extraction, and Retention Forces						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
GBIC insertion	F _I	0		20	Newtons	~4.5 lbs
GBIC extraction	F _E	0		15	Newtons	~3.3 lbs
GBIC retention	F _R	130		N/A	Newtons	Straight out ~29.3 lbs

Table 10. Insertion, extraction, and retention forces

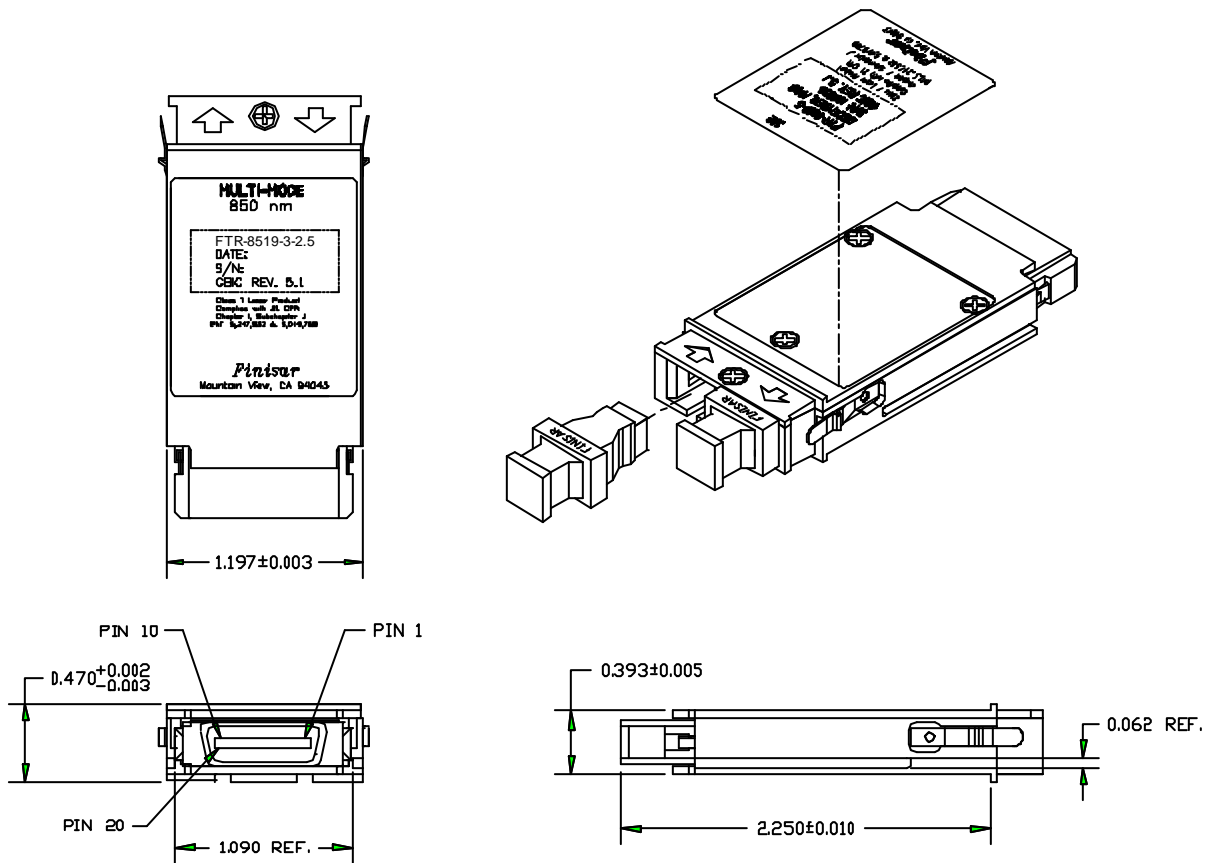


Figure 1. GBIC Outline Drawing

X. References

1. “Gigabit Interface Converter (GBIC) Revision 5.4”. Sun Microsystems Computer Company et. al., August 16, 1999. <http://playground.sun.com/pub/OEmod/>
2. “IEEE Draft P802.3z/D5.0 ‘Media Access Control (MAC) Parameters, Physical Layer, Repeater and Management Parameters for 1000Mb/s Operation’”. IEEE Standards Department, 1998.
3. “Fibre Channel Draft Physical Interface Specification (FC-PI 10.0)”. American National Standard for Information Systems.
4. “Application Note AN-2025: Using the Built in Test/Diagnostics Port”. Finisar Corporation, September 1998. www.finisar.com
5. “AT24C01A/02/04/08/16 2-Wire Serial CMOS E²PROM”. Atmel Corporation. www.Atmel.com

XI. For More Information

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